

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: N. KANEKAWA, et al
Serial No.: Not yet assigned
Filed: February 26, 2004
For: ELECTRONIC CIRCUIT PACKAGE
Group: 2818
Examiner: V. Nguyen

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.97 & 1.98**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

February 26, 2004

Sir:

In the matter of the above-identified application, this Information Disclosure Statement is being submitted with the following citation as specified in 37 CFR §1.97(d).

"A copy of any patent, publication or other information listed in an Information Disclosure Statement is not required to be provided if it was previously cited by or submitted to the Office in a prior application, provided that the prior application is properly identified in the statement and relied upon for an earlier filing date under 35 U.S.C. §120."

Applicant(s) are submitting herewith a copy of Form PTO-1449 which list documents cited in parent application(s) Serial No. 10/370,518, filed February 24, 2003; Serial No. 09/793,968, filed February 28, 2001, now U.S. Patent No. 6,584,004; Serial No. 09/271,448, filed March 18, 1999, now U.S. Patent No. 6,223,273; Serial No. 09/095,049, filed June 10, 1998, now U.S. Patent No.

6,195,742; Serial No. 08/746,942, filed November 18, 1996, now U.S. Patent No. 5,789,805; Serial No. 08/523,346, filed September 5, 1995, now U.S. Patent No. 5,614,761; Serial No. 07/843,234, filed February 28, 1992, now U.S. Patent No. 5,468,992.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (501.30980CC7) please credit any excess fees to such deposit account.

Respectfully submitted,



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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4 7 7 3 0 4 4	9/88	Sfarti et al	711	211	
	4 5 7 7 2 9 3	3/86	Matick et al	365	189.04	
	4 1 7 2 2 8 2	10/79	Aichelmann, Jr. et al	364	246.92	
	5 4 6 8 9 9 2	11/95	Kanekawa et al	257	676	
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	4 4 4 1 1 6 4	4/84	PAVEN, et al.			
	5 2 0 0 8 1 0	4/93	Wojnarowski, et al.			4/5/90
	5 2 4 1 4 5 6	8/93	Marcinkiewicz, et al.			7/2/90
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FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT
					YES NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Synchronous Dram Module; Advance 64 MEG & 72 Registered SDRAM DIMM; pages 1-17.
	19404 - word X 9 - bit High Density Dynamic RAM Module; pages 849-857.

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	5 0 8 1 5 6 3	1/92	Feng et al.			4/27/90
	4 6 0 2 2 7 1	7/86	Dougherty, Jr. et al.			
	4 6 4 9 4 7 4	3/87	Ambrosius, III et al.			
	4 1 4 4 5 6 1	3/79	Tu, et al.			
	5 1 8 2 6 3 2	1/93	Bechtel, et al.			11/22/89
	4 7 8 3 6 9 5	11/88	Eichelberger, et al.			
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	5 1 8 5 7 1 7	02/93	Mori			07/31/89
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	4 8 1 1 2 8 8	3/89	Kleijne, et al.			06/24/86
	4 9 7 9 2 8 9	12/90	Dunaway, et al.			
	4 7 4 6 9 6 6	5/88	Fitzgerald et al.			
	5 1 7 3 8 4 4	12/92	Adachi, et al.			11/19/91
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	4 8 0 7 2 8 4	02/89	Kleijne			06/05/87
	4 9 3 3 8 9 8	06/90	Gilberg, et al.			01/12/89
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	6 2 2 3 2 7 3	4/01	Kanekawa et al	712	33	
	6 1 9 5 7 4 2	2/01	Kanekawa et al	712	33	
2 0 0 1	0 0 2 4 3 8 9	9/01	Funaba et al	365	200	
	6 3 7 6 9 1 7	4/02	Takeshita et al	257	778	
2 0 0 1	0 0 3 3 0 1 3	10/01	Lee	257	679	
2 0 0 2	0 0 5 6 9 1 1	5/02	Iwaya et al	257	738	
2 0 0 1	0 0 2 2 7 3 9	9/01	Funaba et al	365	63	
	6 3 2 4 1 1 4	11/01	Hineno	365	230.03	
	4 7 5 2 9 2 7	6/98	Melling, Jr.	714	3	

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	5 1 4 9 9 4 0	9/92	Davis et al	219	130.21	
	5 0 6 8 8 5 0	11/91	Moore	370	449	
	4 9 2 2 3 6 3	5/90	Long et al	361	3	
2 0 0 2	0 0 4 0 2 6 1	4/02	Nakamoto et al	701	1	
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	5 7 8 9 8 0 5	8/98	Kanekawa, et al			
	6 5 8 4 0 0 4	6/03	Kanekawa, et al			

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